**Energy-Efficient 3-bit Flash ADC with 3 GHz Sampling Frequency and 6.51ns Delay for Wi-Fi 7: Comprehensive Design from Schematic to GDSII in 90nm CMOS Technology**

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**Abstract**

This paper presents a 3-bit flash ADC optimized for Wi-Fi 7, which would require a sampling rate of 2.4 GHz and power consumption below 100 mW to adequately process wideband signals and carry the highly demanding throughput and low-latency demands of future wireless applications. The proposed ADC flashes an impressive sampling rate of 3GHz with an extremely low power consumption, only 1.397 mW. With delay of 6.51ns. Hence, the architecture is very competitive for ultra-low latency applications. It is very low power and low latency and, therefore, apt for low power applications. In addition, the ADC has been synthesized in Cadence 90nm CMOS technology. The paper throws light on the entire design process from schematic development to the generation of a GDSII file so that the fabrication of this architecture is totally demonstrated.

**Keywords:**

Modified Strong-Arm Latch Comparator, Flash ADC, High Speed, GDS-II, Wi-Fi-7

1. **Introduction**

The next generation of wireless communication standards is Wi-Fi 7, which will double the throughput efficiency, cut latency, and significantly boost the efficiency of network infrastructures. Advanced technologies and, more importantly, those that convert analog signals to digital are critical in the conversion of analog signals to digital formats in the management of high data rates and wide bandwidths demanded by Wi-Fi 7. Fast performance makes Flash ADC critical for managing these several high data rates and wide bandwidths provided by Wi-Fi 7.

Flash ADCs, or parallel ADCs, are required to allow for the speeds at which Wi-Fi 7 needs to run. The devices take analog signals, containing all sorts of data that's coming from antennas, and convert them into digital form at extremely high rates. This fast conversion is exactly what is required for effective bandwidth processing; Since Flash ADCs can convert accurately and rapidly, they can process wide bandwidths efficiently and capture subtle changes in signal processing for high fidelity applications.

Besides dealing with the trade-off between speed and resolution concerning power consumption and cost, high sampling rate Flash ADCs in Wi-Fi 7 technology will present further technical challenges to the designer. High-speed, high-resolution ADCs are much more power hungry and expensive, which constitutes a major design challenge when these devices are consumer grade. The second challenge for extreme high frequency concerns the signal integrity at the receiver side, for which advanced filtering and signal processing techniques are required to obtain accurate data conversion and reliable wireless performance.

Thus, to have the practical implementation of Wi-Fi 7, Flash ADCs can be combined with high sampling rates. The Flash ADCs can provide the much needed speed and precision for meeting demands for high bandwidth and data rates in modern wireless systems.

In the designs of flash ADCs for Wi-Fi 7 applications, clock frequency together with power consumption becomes critical contributors to optimal performance. Clock frequency inherently determines the sampling rate, while higher frequencies will permit faster acquisition of data, which is a need for wide channels in Wi-Fi 7 at up to 320 MHz The sampling rates are thus made very high, usually about or even higher than 2 GSps, to digitize the signal with much accuracy prior to transmission. However, an increase in clock frequency may also scale the power consumption, so good balance between performance and energy efficiency is crucial. For portable Wi-Fi 7 devices to get a long battery life and generate minimal heat from a device, less than 100 mW of low power consumption is especially important. It is this balance therefore that will enable high performance without sacrificing portability and use in some of the most power-sensitive applications such as mobile phones, IoT devices, and AR/VR systems.

Signal processing components are increasingly required to be portable and compact, with converters being a prime example of this need [2]. Nevertheless, one of the major disadvantages of the flash ADC is cost, which has a cost scalability that grows exponentially with the resolution. All these factors include power consumption, input capacitance, comparator kickback noise, chip area, and signal routing challenges [1-5].

For instance, a practical example is that of a 3-bit flash ADC that quickly converts analog information into the digital format. Here, this architecture uses a number of comparators in parallel that compare an incoming signal simultaneously against an array of reference voltages which are created based on a resistor ladder network. The output of these comparators is passed through a priority encoder, this information is then translated into a three-bit binary value representing the strength of the input signal

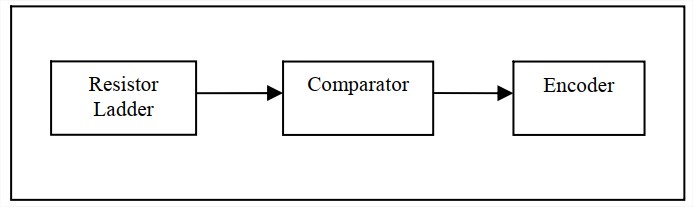
Figure 1 shows a very basic structure of a flash ADC. From the above figure, it can be seen that one of the major parts of ADCs is the comparator, which is commonly known as a 1-bit ADC.[3]

Fig.1 Flash ADC block diagram

Flash ADC consists of three blocks

1. Ladder of resistive networks
2. Comparators
3. Priority Encoder
4. **Ladder of resistive network**

A resistor ladder network is typically made using series-connected resistors, all of the same value. A flash ADC of N-bit have N resistors, all equal to the resistance R. The resistor ladder is connected at one end to the reference voltage and at the other to ground. This configuration causes a progressive alteration in voltage at each level of the comparator.

In an n-bit flash ADC, there are total of n resistors. Since every resistor has resistance R then the network's total resistance equals n \* R. The voltage at each step can be found by a part from total voltage. The following expression can be used to find the voltage drop across each stage

Where m=1,2, 3, n

This is then compared with the analog input applied at that stage by the comparator, resulting in the production of the digital output after each stage.

1. **Comparators**

Comparators have two inputs and output binary values and compare two signals. It has three configurations: Three sections discussed were a basic inverter, an open-loop operational amplifier, and a differential amplifier with a cross-coupled latch [3][12]. Flash ADCs consume more power compared to the comparison done by them. It allows for comparing an analog sine signal with a reference voltage, provided by the resistor network in each stage [12]. The output of a comparator is binary logic 1 if the analog signal is more elevated than the reference voltage. If the analog signal peak is not more than the reference voltage, then the binary output is logic 0. The time that was taken to decide limits these comparators' speed. This is one of the main tasks of the CMOS comparator, the comparison of the signal with the reference and determining whether it is larger or less than the reference signal. the comparator symbol is shown in fig2 below.

1 if

0 Otherwise

Where the analog input is signal [15] and is the reference voltage

Resolution of ADC determines the number of comparators that are required [3]. To find out therequired comparators of an n-bit flash ADC, the formula is as follows:

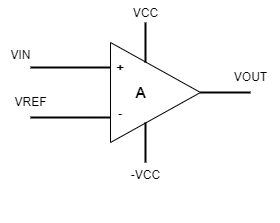


Fig.2.comparator symbol

The different types are the strong-arm latched comparator, modified strong-arm latched comparator, and standard dynamic comparator. Since the modified strong-arm latch comparator consumes low power, it is one of the favorites among the options. The proposed flash ADCs use it. Then, the binary outputs obtained from the comparators are forwarded to the priority encoder module [17].

1. **PRIORITY ENCODER**

In a scenario when many inputs are being processed simultaneously, a priority encoder will prioritize the high-priority bit. The priority encoder is an essential element of the Flash ADC. It transforms the comparator's output into the digital binary code corresponding to the provided analog input.

In a flash ADC, each comparator generates a binary signal indicating whether the analog input exceeds a reference voltage. The output of all the comparators produces a binary sequence, in which a "1" indicates that the input is more than the reference, and a "0" indicates that the Vref is greater than the input voltage.

It is required to have a set of eight comparators. Since the comparator outputs 8 digital values, the priority encoder takes these 8 output values of comparator as input the 8 to 3 priority encoder. For flash ADCs to carry out efficient and quick data conversion in a space-saving way, the technique is vital

The 8 to 3 priority encoder's circuit design is shown in Figure 3 [16]. 'D0,' 'D1', 'D2', 'D3', 'D4', 'D5', 'D6', and 'D7' are the digital bits that the comparator inputs into the encoder. The most important bit, D7, is always connected to the earth, whereas the least important bit, D0, is always linked to nothing. The results are represented by the bits "Q0" and "Q2," which are the Most Significant Bit (MSB) and Least Significant Bit (LSB), respectively [35].

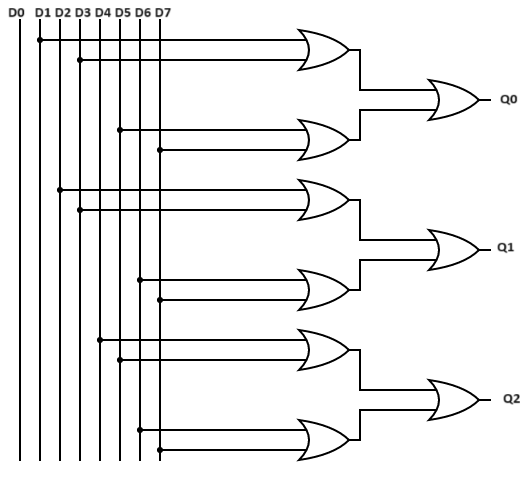


Fig.3. Logic diagram of Priority encoder

1. **IMPLEMENTATION OF FLAH ADC.**

The first step of the flash ADC incorporates a resistive network, as seen in Figure 4. During this step, a predetermined voltage is provided to the network of resistors. Every resistor step undergoes a voltage decrease, which is then compared to the input signal.

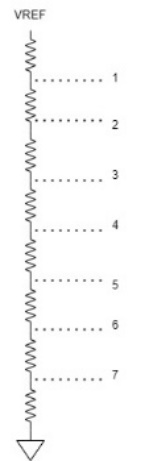
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Fig.4. Resistive network ladder

Fig. 4 depicts a resistive network consisting of 8 resistors, each with a resistance of R. The voltage drop at the first point is 7/8Vref, at the second point, it is 6/8 Vrefand at the third point, it is 5/8 Vref, and so on. Finally, at the last stage, the voltage drop is 0/8 Vref, which is connected to the ground. The voltages at each step are linked to the inverting terminal of the Modified strong-arm latched comparator. In addition, an analog input is connected to the non-inverting input [24].

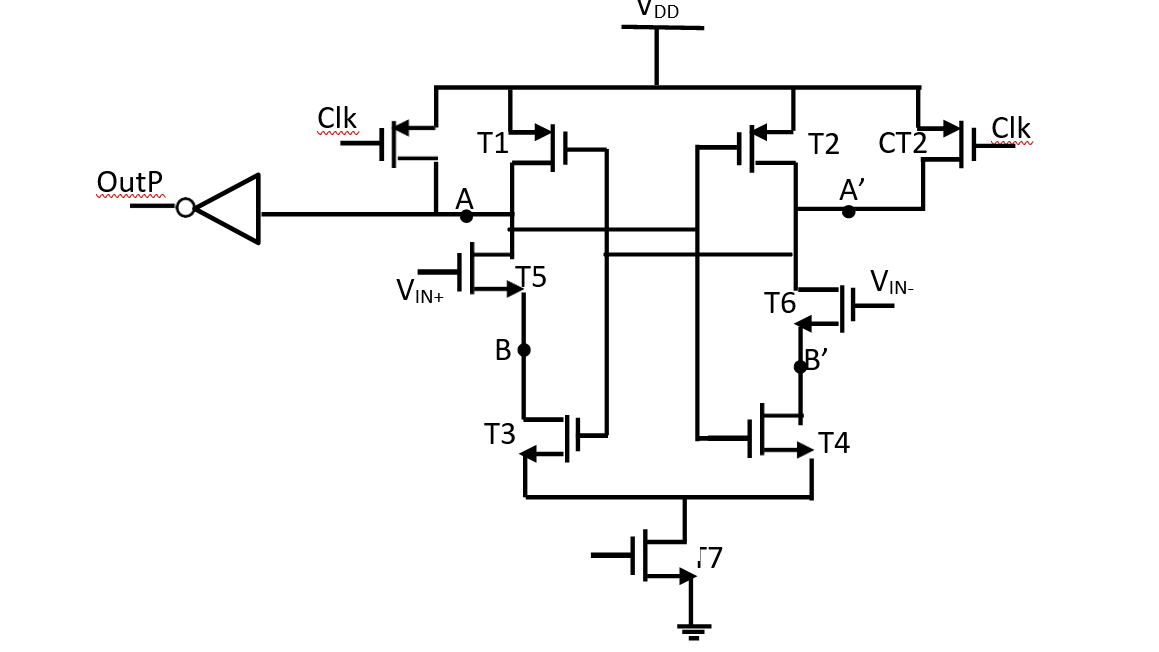


Fig.5.structure of Modified strong arm latched Comparator

Figure 5 shows the modified strong arm latch comparator's CMOS architecture. The non-inverting terminal in this configuration is T5, while the inverting terminal is T6. In this circuit, T6 is the reference signal and T5 is the analog input signal that is connected to the gate.

In the first stage of the comparator, the non-inverting input is determined by the analog input signal, while the inverting input is determined by the7/8 Vref. The comparator evaluates the two input signals and produces the results in the following way.

1 if

0 Otherwise

Similarly, the Stage-II compares the input signal with and the output is as follows

1 if

0 Otherwise

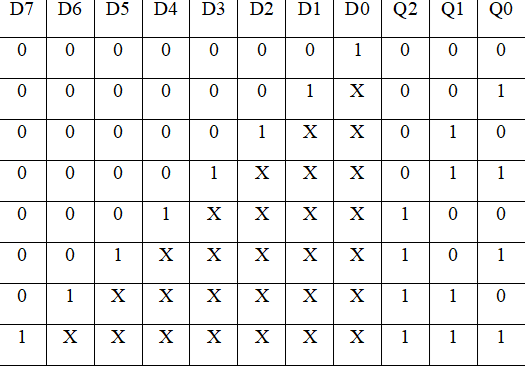
The priority encoder utilizes the analogue input signal to compare the succeeding stages with their respective reference values, producing a binary output the binary output is thereafter inputted into the priority encoder for digital encoding.

The priority encoder receives input from the comparator stage over eight channels: ‘D0’, ‘D1’, ‘D2’, ‘D3’, ‘D4’, ‘D5’, ‘D6’, and ‘D7’. ‘D7’ is assigned the greatest priority, whereas ‘D0’ is assigned the lowest priority and is consistently connected to the ground. These three-bit ‘Q0’, ‘Q1’, and ‘Q2’ dictate the encoder's output. Here the ‘QO’ is the LSB and ‘Q1’ is MSB.

The first 4-input OR gate takes inputs 'D1', 'D3', 'D5', and 'D7'. If any of the inputs 'D1', 'D3', 'D5', or 'D7' is high, then the output will be, that is 'Q0' will be high else it will remain low. The second 4-input OR gate is linked to inputs 'D2', 'D3', 'D6', and 'D7'. The output is 'Q1', which increases if any of the inputs ('D2', 'D3', 'D6', or 'D7') is elevated. In the absence of elevated readings, 'Q1' is deemed low. The third OR gate, which has four inputs, is connected to ‘D4’, ‘D5’, ‘D6’, and ‘D7’. The gate produces an output labelled 'Q2', which becomes high if any of the four inputs (‘D4’, ‘D5’, ‘D6’, or ‘D7’) are high. If none of these inputs have a high value, then the output 'Q2' has a low value.

The priority encoder is specifically intended to assign the highest priority input among D7 through D1 to determine the values of Q0, Q1, and Q2. In this arrangement, Q2 corresponds to the more significant bits, whereas Q0 catches the less significant bits. The ultimate result is that the most important input is transformed into a 3-bit binary representation.

Table 1: Truth table of priority encoder





1. **RESULTS AND DISCUSSION**

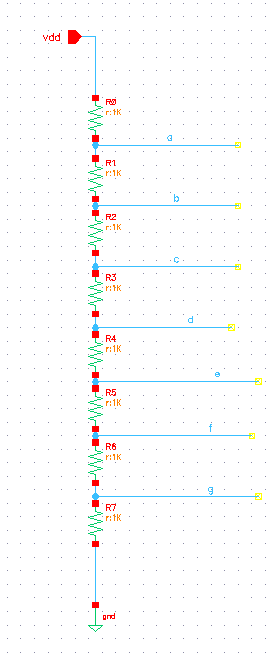


Fig.6. Schematic of the resistive ladder in cadence 90nm

Figure 6 illustrates the resistive network component of the 3-bit flash ADC. The system consists of 8 resistors, each having a resistance of 1KΩ. The maximum reference voltage is 1.75 volts, and it is connected to the ground at the lower terminal. The following table presents a comprehensive analysis of the voltage decrease across each resistor

Table 2 Reference voltages at different nodes

|  |  |  |
| --- | --- | --- |
| a |  | 1.53125 |
| b | = 1.75 | 1.3125 |
| c | = | 1.09375 |
| d | = | 0.875 |
| e | = | 0.65625 |
| f | = | 0.4375 |
| g | = | 0.21875 |
| h | = | 0 |

The inverting terminal of the comparator receives these specific voltages at that particular step, with a reference voltage of 1.75V.

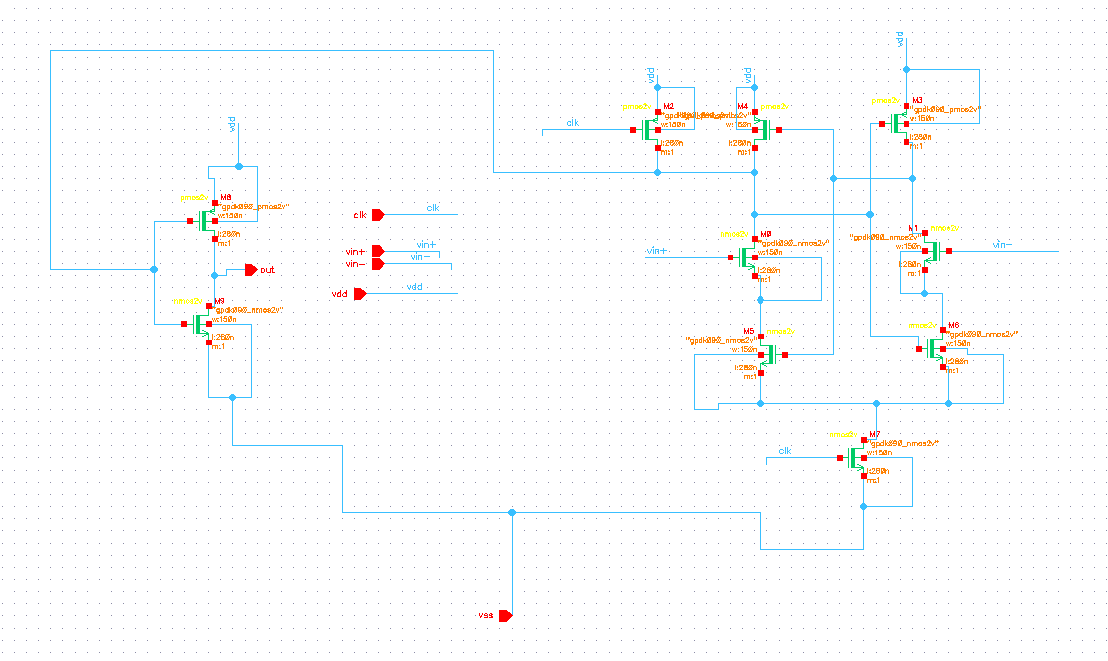
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Fig.7. Schematic of strongarm latched comparator in cadence 90nm

Figure 7 depicts an improved and resilient latch comparator that is specifically designed and simulated using Cadence Virtuoso 90nm technology. The analog input signals are used as Vin+ and Vin-. Vin+ is used to receive the analog input signal, whereas Vin- is supplied with the reference voltage Vref at that specific step. The results of the comparison provide a logic '1' or a logic '0'. When the clock signal is in its high, the tail comparator is activated, enabling the passage of current. If the conductivity is high, the current passing through that node will be substantial, resulting in significant voltage drops across the nodes on that side. As a result, the PMOS transistors that are linked between these nodes will activate before anything else and restore the output to the voltage level of VDD. The comparison is conducted at each iteration by using their corresponding values, together with the given analog input, leading to the production of a thermometer code. The priority encoder is used to generate the digital output once the temperature measurement code is supplied.

The logic architecture shown in Figure 8 illustrates an 8:3 priority encoder. The inputs ‘D7’, ‘D6’, ‘D5’, ‘D4’, ‘D3’, ‘D2’, and ‘D1’ are derived from the comparator stage, while the digital output is represented by the outputs ‘Q0’, ‘Q1’, and ‘Q2’.

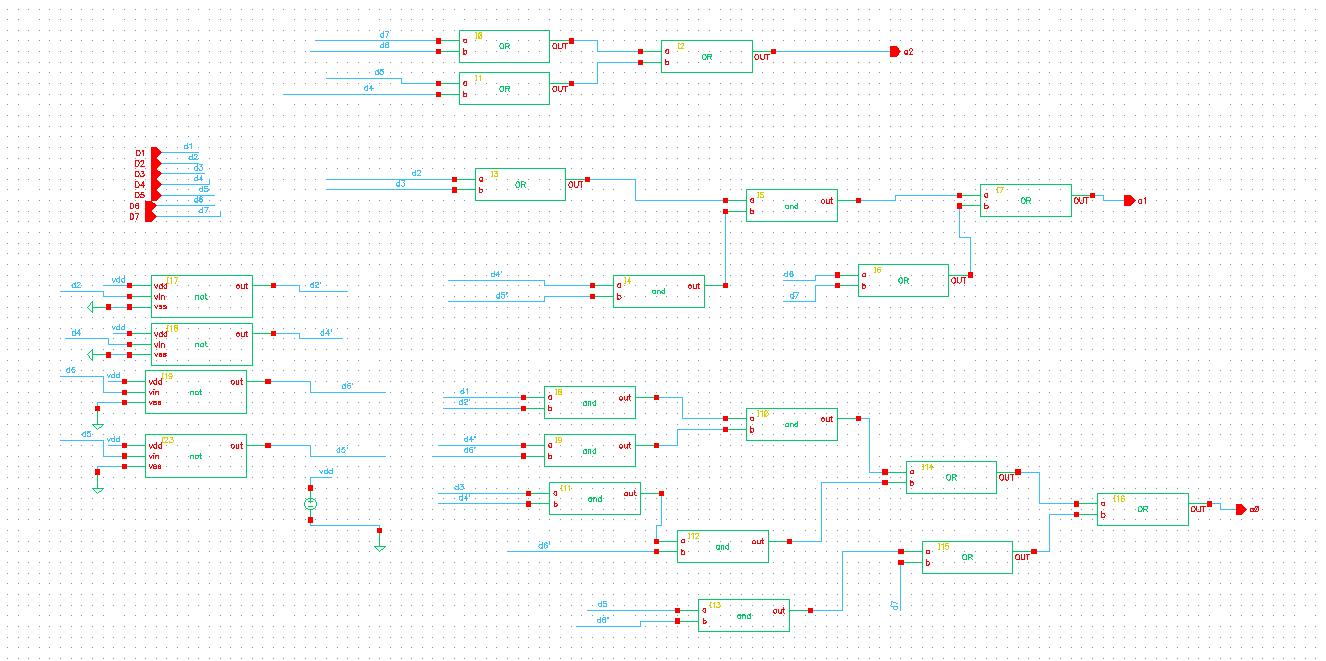


Fig.8. Schematic of 8:3 priority encoder in cadence 90nm

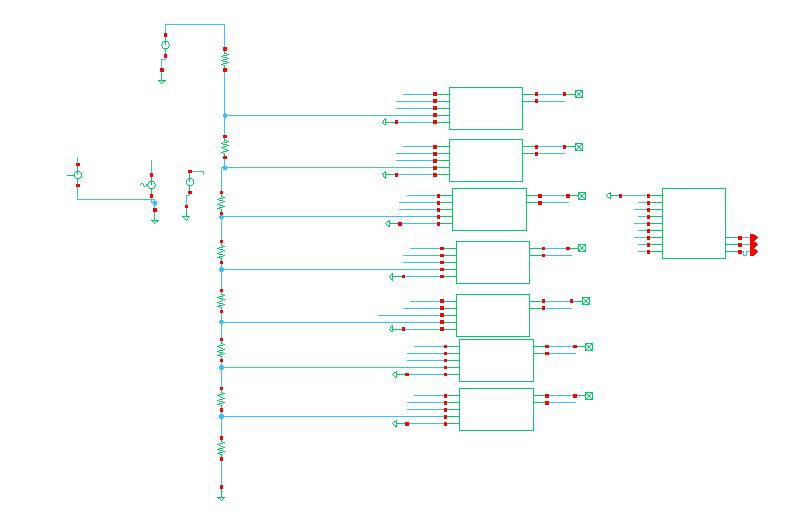


Fig.9. Schematic of FlashADC(3-bit)

Figure 9 shows the schematic of a 3-bit Flash Analog-to-Digital Converter (ADC), including 8 resistors that are coupled in a series configuration, with each resistor having a resistance of 1KΩ The comparator uses the voltage drop across each resistor as the reference input, while the non-inverting terminal gets an analog signal with an amplitude of 1.5V.

Assuming that each comparator consists of one stage, we will have a total of 7 stages. Each stage will provide a binary output, either logic 1 or logic 0, depending on the comparison.

Table 3: Supply parameters for output of 101

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | frequency |  | Clock voltage | Clock frequency |
| 1.238 V | 50MHz | 1.75V | 2V | 3 Giga samples/sec |

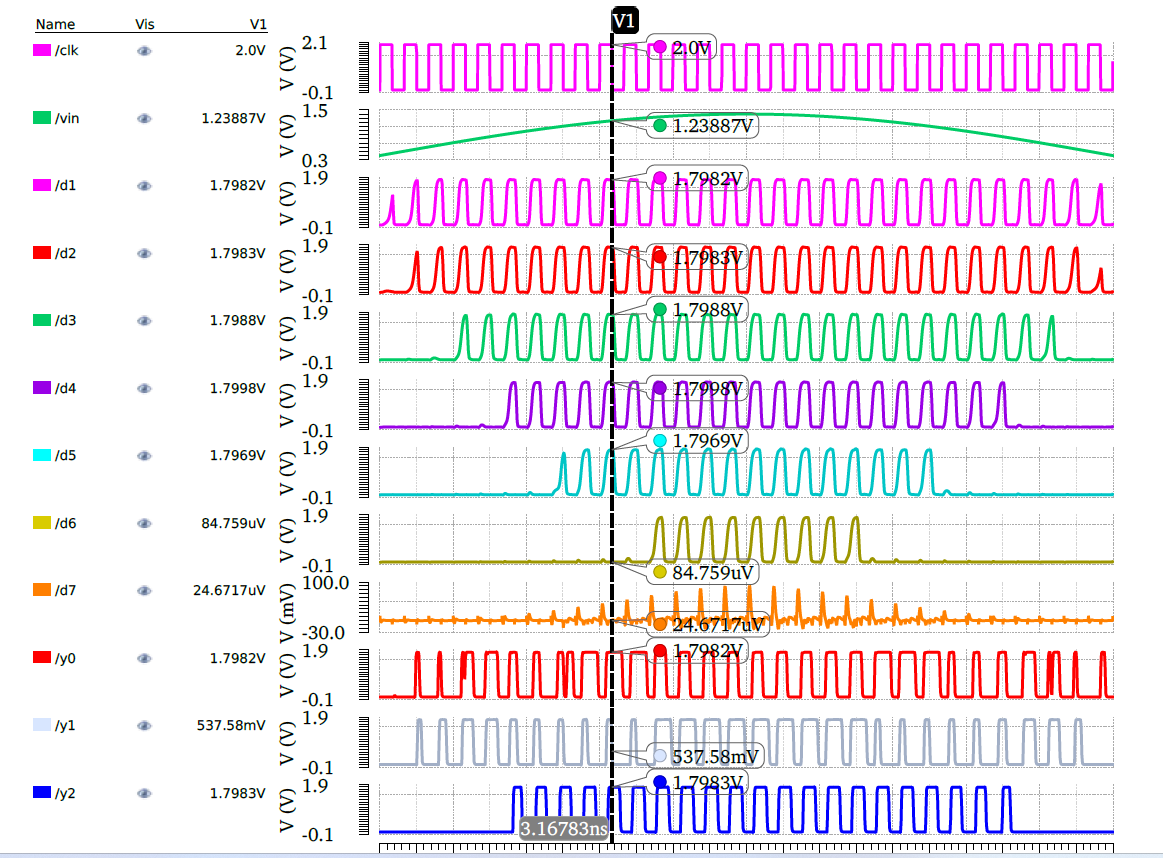


Fig.10. Output of ADC at an input of 1.23887V

The 50 MHz sinusoidal wave with an amplitude of 1 V represents the input analog signal, as seen in Figure 10. Our emphasis is on a specific voltage point of 1.2388V, with a sampling rate of 3G samples per second

Table 4: Comparator output at various stages

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Stages | The reference voltage at a particular stage |  | Comparison phase | Comparator  Analog output | Comparator  Digital  output | Input of priority encoder |
| Stage-I | 1.53125 | 1.2388V | > | 24.6717µV | 0 | D7 |
| Stage-II | 1.3125 | 1.2388V | > | 84.759µV | 0 | D6 |
| Stage-III | 1.09375 | 1.2388V | < | 1.796V | 1 | D5 |
| Stage-IV | 0.875 | 1.2388V | < | 1.799V | 1 | D4 |
| Stage-V | 0.65625 | 1.2388V | < | 1.798V | 1 | D3 |
| Stage-VI | 0.4375 | 1.2388V | < | 1.798V | 1 | D2 |
| Stage-VII | 0.21875 | 1.2388V | < | 1.798V | 1 | D1 |

Table 4 indicates that the input voltage is 1.2388V, while the reference voltage at Stage-I is 1.53125V. The comparator performs a comparison between a voltage of 1.2388V and a voltage of 1.53125V. Since the magnitude of 'A' is bigger than 'B', the resulting output decreases to Vss. In Stage-II, the comparator evaluates the input voltage, which remains constant at 1.2388V, against the reference value of 1.3125V in stage II. As a result, the output decreases to the steady-state value (Vss) since the input voltage surpasses the reference value.

In Stage III, with the input voltage at 1.2388V and the reference voltage at 1.09375V, since is less than, the output enters the regeneration phase and reaches Vdd, resulting in logic 1. Similarly, in Stages IV, V, VI, and VII, considering that the voltage input is higher than the voltage reference (<), they produce logic 1 as output.

The binary outputs of the comparator serve as the input for the priority encoder [16]. The inputs of the priority encoder are composed of multiple bits, where the D7 bit holds the highest priority and the other bits hold lower priority. Given that D7 and D6 are both 0, and D5 is a logic 1 from the output of Stage-III, the digital output y2, y1, and y0 are '1', '0', and '1', respectively, irrespective of the remaining low-priority bits. Figure 9 illustrates this

Table 5: priority encoder output

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **y2** | **y1** | **y0** |
| 0 | 0 | 1 | X | X | X | X | X | 1 | 0 | 1 |

Table 6: Supply parameters for the output of 011

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | frequency |  | Clock voltage | Clock frequency |
| 750.534mV | 50MHz | 1.75V | 2V | 3 Giga samples/sec |

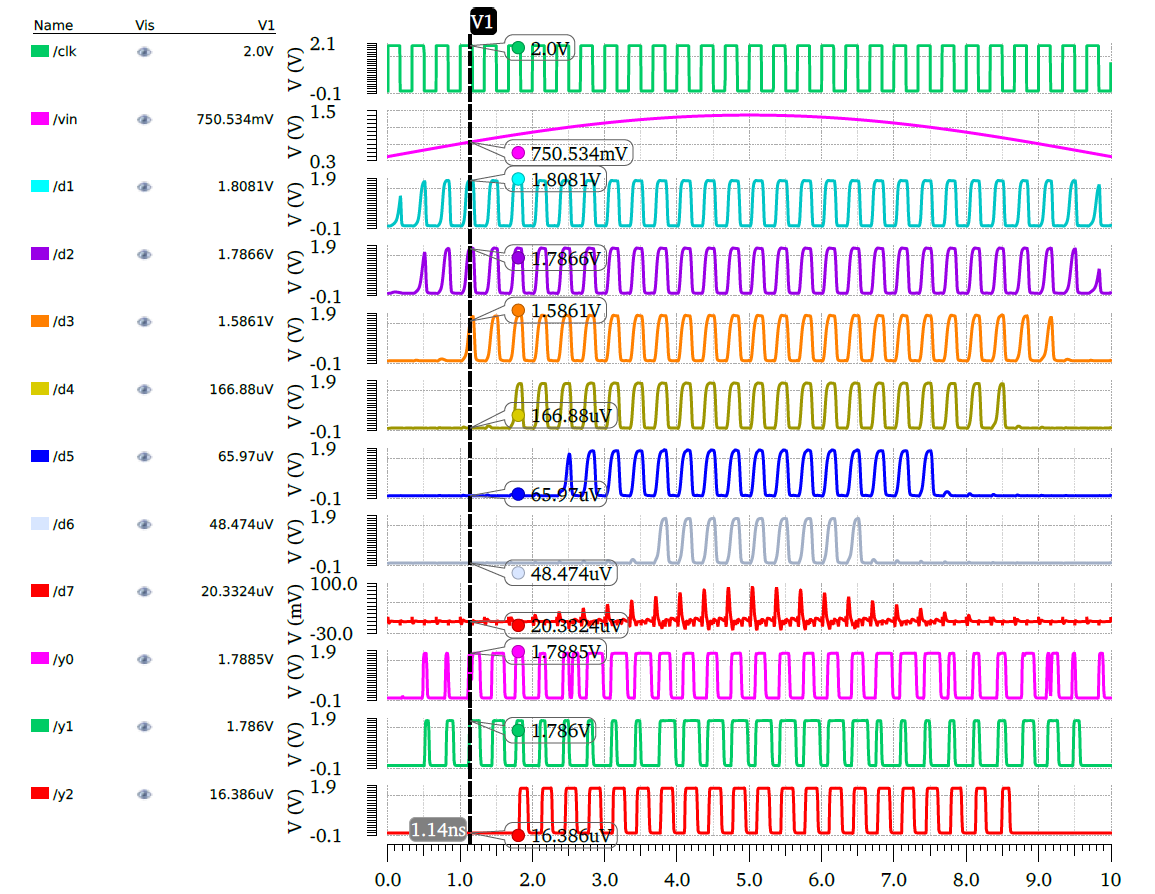


Fig.11. Output of ADC at an input of 750.534mV

Table 7: Comparator output at various stages

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Stages | The reference voltage at a particular stage |  | Comparison phase | Comparator  Analog output | Comparator  Digital  output | Input of priority encoder |
| Stage-I | 1.53125 | 0.750V | > | 20.3324µV | 0 | D7 |
| Stage-II | 1.3125 | 0.750V | > | 48.474µV | 0 | D6 |
| Stage-III | 1.09375 | 0.750V |  | 65.97µV | 0 | D5 |
| Stage-IV | 0.875 | 0.750V |  | 166.88µV | 0 | D4 |
| Stage-V | 0.65625 | 0.750V | < | 1.5861V | 1 | D3 |
| Stage-VI | 0.4375 | 0.750V | < | 1.7866V | 1 | D2 |
| Stage-VII | 0.21875 | 0.750V | < | 1.808V | 1 | D1 |

In Stage I, the Vref is 1.53125V, and the Vin is 0.750V, as shown in the table above. As is greater than the output of the comparator discharges to vss. Similarly, for Stages II, III, IV the Vref is greater than vin so the output of the comparator discharges to vss. At the stage V the Vrefi.e 0.65625V is less than Vin i.e. 0.750V so the output of the comparator reaches to VDD.

As D3 is high and D7, D6, D5, D4, are low the output of the priority encoder should be 011 as shown in Fig.10

Table 8: output of priority encoder for output 011

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Y2** | **Y1** | **Y0** |
| 0 | 0 | 0 | 0 | 1 | X | X | X | 0 | 1 | 1 |

1. **PHYSICAL VERFICATION**

Drawing the layout and doing a DRC and Layout versus Schematic check are the subsequent steps after the schematic simulation. After the design goes through the DRC and LVS, the parasitic capacitance is extracted.

1. **Design rule check**

After the schematic simulation is finished, the next step is to generate the layout and perform DRC andLVS verification. Once the layout has passed the above rule checks, it proceeds to extract the parasitic capacitance. Then, a GDS-II file is generated and then transmitted to the foundry for manufacturing.

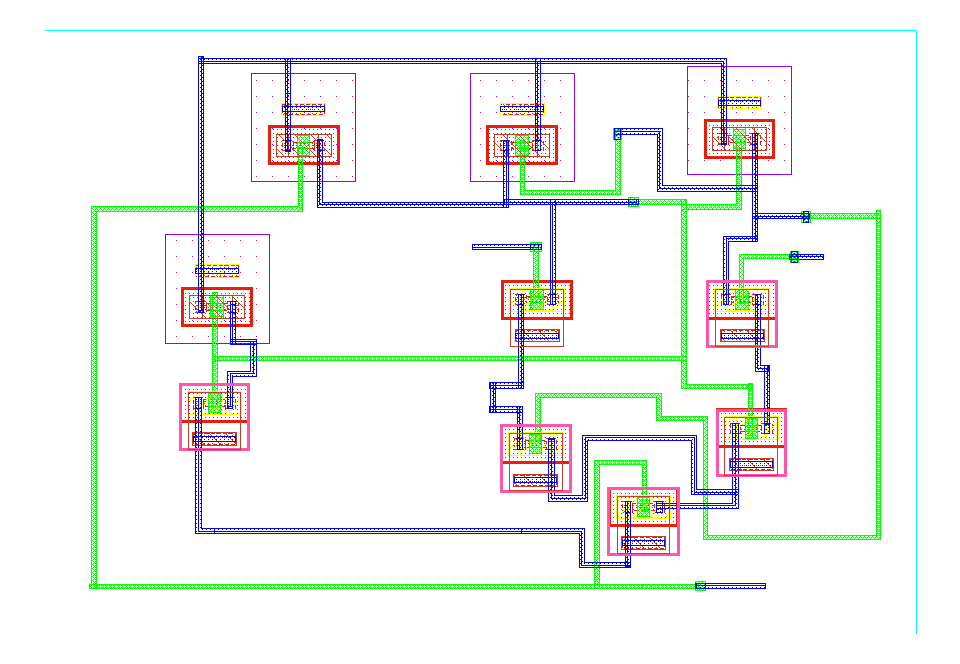


Fig.12. Layout of the Modified strongarm latched comparator

Figure 12 shows the layout for the schematic of the Modified Strong arm latched comparator in Fig. 7. Subsequently, the output from the comparators is sent into an 8:3 priority encoder.

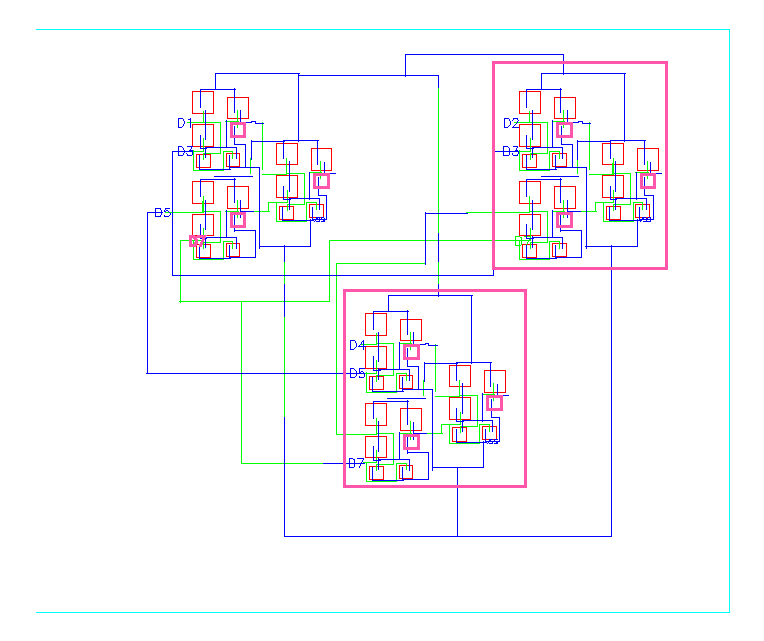


Fig.13. Layout of the 8:3 priority encoder

The layout for 7 comparators and an 8:3 priority encoder is shown below. Fig. 14 shows that the layout successfully passed the DRC the next step is to perform the LVS rule check.

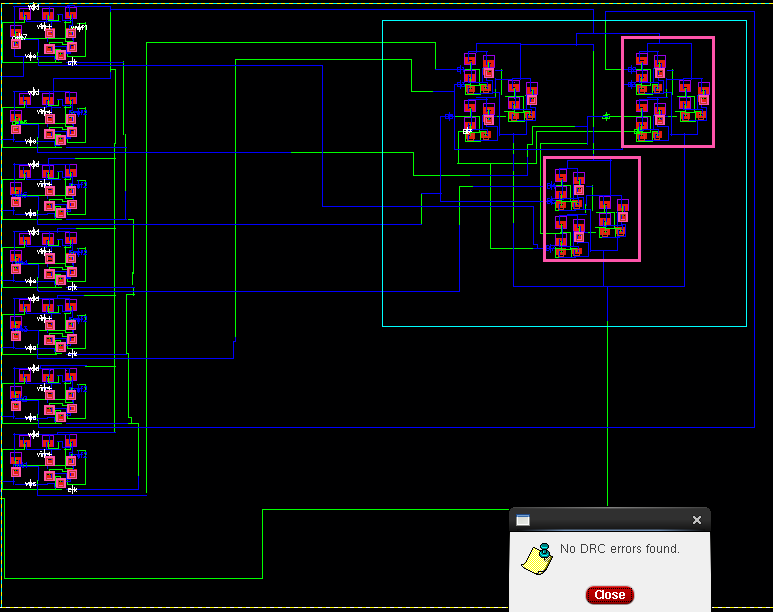


Fig.14 Layout of the Flash ADC (3-bit)

1. **LVS**

Figure 14, the 3-bit Flash ADC has successfully passed all Design Rule Checks (DRC), confirming its compliance with the manufacturing process rules and limits. Consequently, the design is now prepared for Layout Versus Schematic (LVS) inspections, which verify that the actual layout accurately corresponds to the initial schematic.

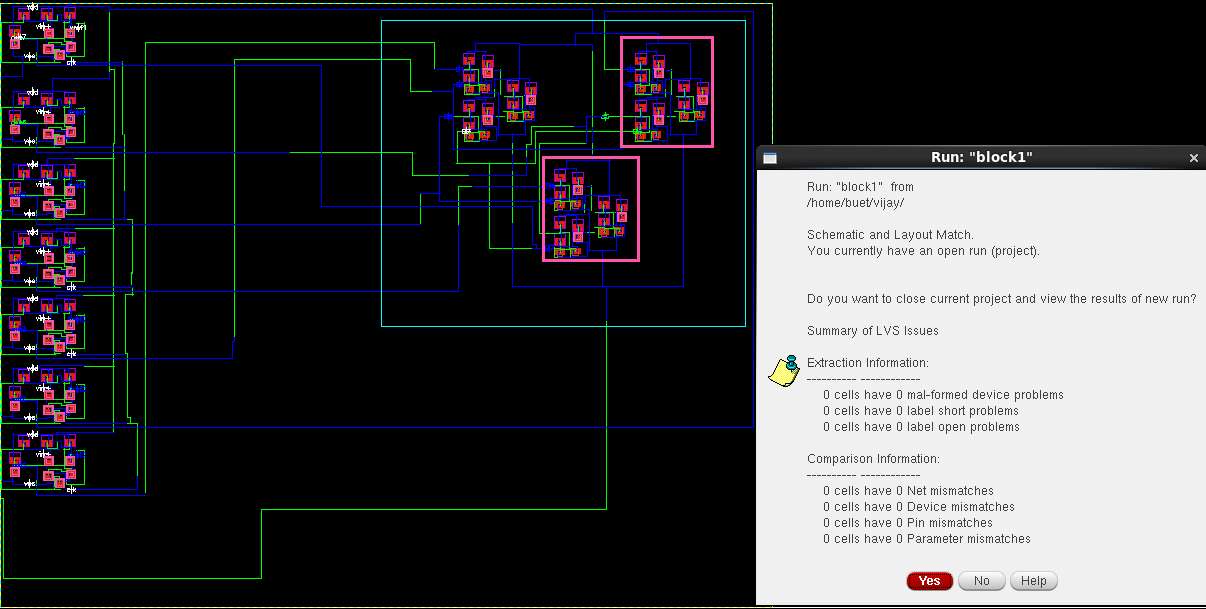


Fig.15 LVS report for the Flash ADC (3-bit)

Figure 15 displays the LVS report for the Flash ADC, indicating that all pins and nets are precisely aligned with the schematic.

1. **RC-EXTRACTION**

Following a clean LVS pass, the next step is to eliminate parasitic capacitance from the design. Figure 16 displays the AV or Extracted view of the 3-bit flash ADC.

The AV or Extracted view is a simplified version of the layout that includes the essential details needed for further analysis. It typically consists of i. Parasitic elements ii. Connectivity information iii. Simplified geometry.

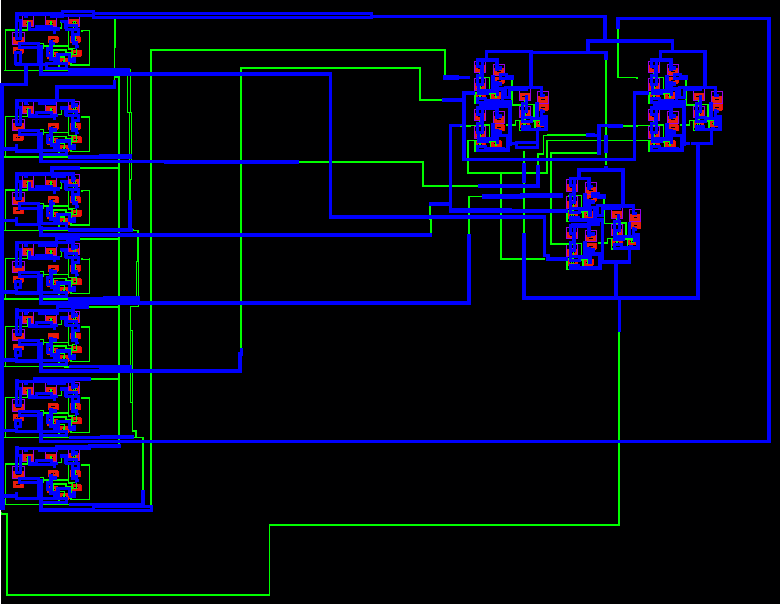


Fig.16 AV or Extracted view of 3-bit flash ADC

1. **GDS-II FILE GENERATION**

After the parasitic capacitance has been removed, the next procedure involves creating a GDS-II file that includes the IC layout specifications. After that, the foundry receives this file and fabricates it.

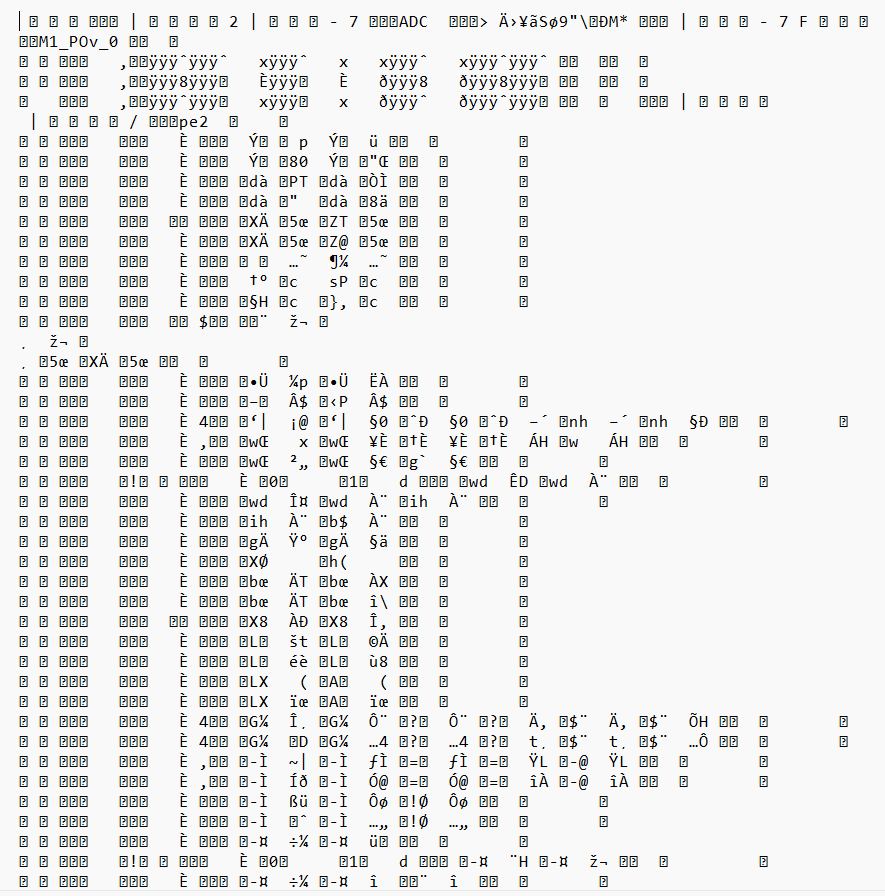


Fig.17. GDS-II file

The fig.17 shows the GDS-II file of the flash ADC which is in unreadable format is sent to the foundry

Table 9: Obtained values for 3-bit flash ADC

|  |  |
| --- | --- |
| **Specifications** | **Range/vlaue** |
| Technology | 90nm |
| Reference voltage | 1.75V |
| Sampling frequency | 3G Samples/sec |
| Supply voltage | 1.8V |
| Input frequency | 50MHz |
| Area | 166.47µX 130.06µ |
| Power | 1.397mW |
| Delay | 6.513ns |

The flash ADC, designed using 90nm technology, operates at a supply voltage of 1.8V and a sampling frequency of 3GHz. It dissipates a power of 1.397mW and has a delay of 6.513nsec, as illustrated in Figure 19. (a) and (b) represent the respective characteristics. The designed Flash ADC has a layout area of 166.47µm X 130.06µm.

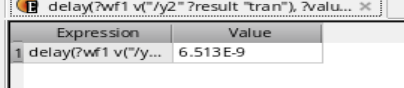
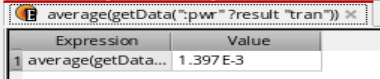


Fig. 19. (a) Power; (b) delay

1. **CONCLUSION**

The proposed 3-bit flash ADC presents an excellent compromise between high sampling rates, low power consumption, and minimal delay. Thus, it is well-suited for future wireless applications, such as Wi-Fi 7. In fact, considering the sampling rate of 3 GHz; a power consumption of only 1.397 mW, and a delay of 6.51ns, the demands of low-latency and low-power applications are strictly met. Thus, the successful realization in 90nm CMOS technology demonstrates its on-field feasibility and has been applied from the schematic level up to GDSII.

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